REMARKS

This communication is a request for reconsideration fully responsive to the Office Action dated July 25, 2008 and received in this application. Reconsideration and allowance of the pending claims in light of the following remarks is respectfully requested.

Claims 1-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 6,332,661 to Yamaguchi ("Yamaguchi") in view of U.S. Pat. No. 7,180,496 to Koyama et al. ("Koyama"). This rejection is traversed.

Claim 1 recites: *[a] current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas,*

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object, each driver comprising

an output means for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object and

a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.

These claimed features are neither disclosed nor suggested by the relied-upon references. Yamaguchi discloses a constant current driving semiconductor integrated circuit configured to drive several loads by using a reference current generating circuit that is embedded to derive a reference output current generated on a reference resistance from a reference output terminal. This provides constant current driver ICs that are intended to operate in a state of small variations in output currents. Applicant submits that this arrangement is similar to that described in Applicant's background of the invention, and is clearly distinct from and not suggestive in any way of Applicant's claimed invention.

There are thus various claimed features that are absent from Yamaguchi. For example, the Action readily admits that, and Yamaguchi makes no mention of, "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means*," as claimed by Applicant.

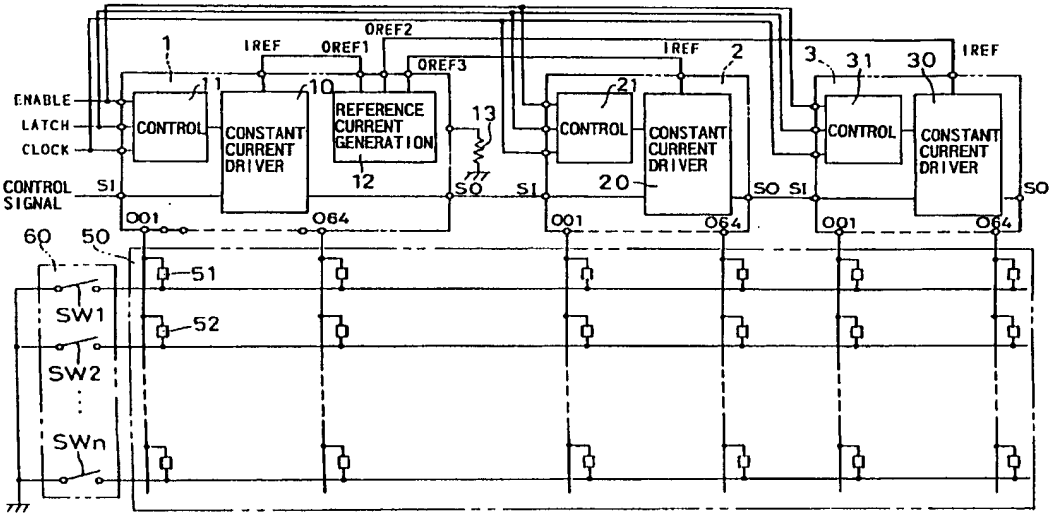
Koyama does not remedy the deficiencies of Yamaguchi. Koyama discloses a drive circuit for driving a liquid crystal display device. Koyama discloses a line driver circuit that outputs digital values (D1, D2, D3) to the pixel array in the form of a voltage. This digital line driver circuit of Koyama fails to even generally disclose the type of circuit claimed by Applicant, which is a "*current output type drive circuit for outputting a drive current ...comprising a plurality of drivers ... for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object.*"

Moreover, like Yamaguchi, Koyama clearly fails to disclose or suggest "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means*," as claimed by Applicant. The Action cites FIG. 2, elements 201 and 202 as a purported example of this feature. However, these elements merely accommodate a latching of a digital signal (D1, D2, D3) that is then provided to a pixel circuit 205. At best, even if this is construed as "sampling" and "holding", the passing of a digital value D1, D2, or D3 to another circuit is clearly not an example of sampling a reference current input from a reference current input terminal. The passage cited in the Action (9:21-25) merely confirms that Koyama samples digital data, and in no way discloses or in any way suggests a reference current source circuit that samples and holds the reference current input from a reference current input terminal, and then supplies the same to the output means.

Additionally, and contrary to the conclusory remarks of the Examiner that sampling and holding signals is a known technique and that this combination would have been obvious, one of ordinary skill in the art would not have combined the claimed elements by known methods as there would be no technical impetus whatsoever to make the modifications consistent with Applicant's

claimed invention, and there would thus also be no expectation that success would result in adding such features to the circuitry of Yamaguchi.

FIG. 1 of Yamaguchi illustrates the current driving circuitry disclosed therein:



Yamaguchi also describes circuitry that provides a current mirror circuit including transistors configured to produce reference current outputs OREF1-3 that have small variations in current value. (See FIG. 3 of Yamaguchi). It would make no technical sense whatsoever to sample and hold these currents in the Yamaguchi circuitry, as these currents are intended to drive loads (with the alleged small variation in current). If one were to sample and hold the OREF1-3 currents, in lieu of using them to drive loads, the circuitry would be rendered completely non-functional.

The reference to FIG. 2 of Yamaguchi (Office Action, at p. 21) as further evidence of the propriety of the combination only further highlights the specious nature of the rejection. Although the explanation in the reference is scant, the register and latch disclosed therein are apparently control circuitry used to determine which line the drive current is to be applied to. This has nothing to do with sampling or holding the value of the actual current.

Accordingly, Yamaguchi discloses circuitry for producing several drive currents with small variation, and Koyama discloses an entirely different type of circuit and fails to disclose or in any way suggest the claimed features that the Action admits are absent from the Yamaguchi reference. The line (voltage) driver circuit by Koyama is a clearly distinct from the current driver circuit claimed by Applicant. Additionally, as noted above, there would be absolutely no reason to even consider sample and hold circuitry in the Yamaguchi circuitry. An ordinarily skilled artisan would in no way look to the latching of a digital value (D1-D3) for application to a line in a pixel circuit to solve problems presented in the current drive circuitry of Yamaguchi. Regardless, a *prima facie* case of obviousness remains absent from the record as even the combination of references would still fail to yield the features of Applicant's claimed invention, namely "*a reference current source circuit for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.*"

For these reasons, the combination of references is thus deficient generally, and the faulty combination still fails to produce the features recited in Applicant's claim 1.

Claims 3-6 depend from claim 1 and thus incorporate the features recited therein. These dependent claims are thus patentably distinct from the relied-upon references for their incorporation of the features of claim 1 as well as for their own, separately recited patentably distinct features.

The position with regard to these claims in the Action only further illustrates the impropriety of the combination as well as the deficiencies of the references, even in combination.

For example, claim 3 recites: ... *said current sampling circuit includes a first current memory and a second current memory, and said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory.* The Action cites elements A1 to A3 and B1 to B3 as the first current memory and elements C1 to C3 as the second current memory. However, as noted, these elements are part of the pixel, not a part of the line drive circuit. It is clear

that these features are not an example of first and second current memories in a current sampling circuit, let alone those that alternately perform write and read operations as claimed. Again, Applicant's claimed invention provides two memory circuits to write and read the reference current in the reference current source circuit, not within the pixel array. The second current memory C1-C3 is merely a non-volatile memory that stores the values in the given pixel when power to the display is cut off, so that the display can automatically display something when it is turned back on. The other elements A1 to A3 and B1 to B3 are merely faster, volatile memories for accommodating a refresh of the display. It is difficult to see how the cited features of Koyama have anything at all to do with the features recited in Applicant's claim 3.

Still further, with regard to claim 4, the relied-upon references offer no disclosure or suggestion of means for increasing the reference current read from the current memory via distribution by time division. It is not sufficient to state that time division is known, as there would be no reason to distribute reference currents by time division in the Yamaguchi reference. With regard to claim 5, there is clearly no disclosure or suggestion of the additional features for carrying out such an operation as clamed. Applicant objects to the unsupported conclusory statements that these claimed features are obvious.

With regard to claim 6, there is also absolutely no discussion in Yamaguchi, as alleged in the Action, of distributing the reference current to the drivers in a vertical blanking period, or of using as the reference current the current held after the vertical blanking period in which digital noise is generated, as claimed by Applicant. Even assuming that Yamaguchi column 6, lines 22-45 discloses the usage of clock signals to control displayed information, there is no mention or suggestion of any kind of distributing the reference current to the drivers in a vertical blanking period. It would also make no sense to do this in Yamaguchi as that circuitry provides drive currents for driving loads. There is no way one would in any way think that it would be "inherent" to distribute the reference current in a vertical blanking period, as this would be non-functional in the Yamaguchi reference. Applicant objects to the unsupported conclusory statement that these claimed features would have been obvious.

Accordingly, claim 1 is clearly distinct from the relied upon references, whether they are taken alone or in any combination. Independent claim 22 is distinct from the relied upon references for reasons similar to those provided regarding claim 1.

Independent claim 7 recites: *[a] current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas,*

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object,

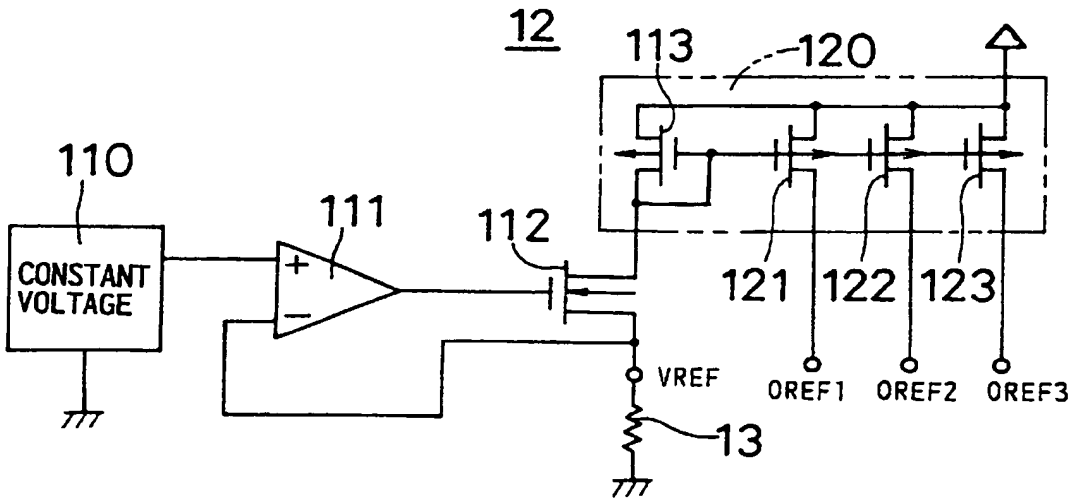
each driver comprising an output means for outputting a supplied reference current as a drive current to the corresponding shared area of the driven object and a reference current source circuit for sampling and holding a reference current input from a reference current input terminal, then supplying the same to the output means,

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect, and

the reference current being distributed to the reference current source circuits of the drivers by time division.

Claim 7 is distinct from the relied-upon references for the reasons noted regarding claim 1 above. Additionally, there is no disclosure or suggestion in the relied upon references of (1) connecting the reference current inputs according to a common current interconnect, or of (2) distributing the reference current to the reference current source circuits of the drivers by time division. As explained above, Yamaguchi discloses a reference current generating circuit that is embedded to derive a reference output current generated on a reference resistance from a reference output terminal. FIG. 3 of Yamaguchi discloses its reference current generating circuit, which is explicitly described as producing different currents for the different current driver circuits.

FIG. 3



This is not an example of the common current interconnect claimed by Applicant. In any event, there is clearly no distribution of the reference current to the reference current source circuits of the drivers by time division, nor is there anything that could coherently support a conclusion that there is any hint or suggestion in that regard. The use of time division appears wholly inappropriate to the circuitry of Yamaguchi, and it is unclear how or if Yamaguchi's drive circuitry would function under such a scenario. In any case, there is clearly no indication whatsoever that time division would be used in the context or fashion claimed by Applicant. It is wholly insufficient to merely conclude that time division is known, and that therefore it would be obvious. Koyama also fails to disclose or in any way suggest such features. The passage cited in the Action, spanning lines 1-21 in column 10, discloses a gray scale technique, which also clearly does not disclose or suggest the claimed features.

Claim 23 is distinct for at least reasons similar to those provided regarding claim 7 above. The remaining claims depend from these claims and are thus distinct for incorporating the features therein as well as for their separately recited, distinct features, some of which are specifically addressed above.

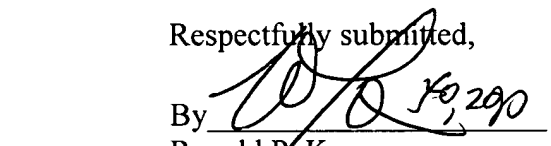
Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-28 under 35 U.S.C. § 103(a) as being unpatentable over Yamaguchi in view of Koyama.

For the record, Applicant appreciates the citation of evidence relating to the prior taking of Official Notice, but does not admit that the corresponding rejection of the claims has merit in this regard. Applicant reserves the right to challenge the propriety of the rejection of claims based upon Official Noticed facts as well as the corresponding evidence.

This response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments supporting the patentability of the claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests the Examiner to provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Dated: September 22, 2008

Respectfully submitted,

By 

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